ABSTRACT OF THE DISCLOSURE

Memory apparatus having a short word line cycle time and method for operating a memory apparatus. One embodiment provides a memory apparatus comprising at least one cell array having a multiplicity of memory cells, with each of the memory cells having an associated word line and an associated bit line; a control device which has a signaling connection to the word lines and to the bit lines and is configured to read data stored in the memory cells and to write data to the memory cells; wherein the control device is configured to execute a destructive read command (DRD) for reading data from at least one of the memory cells, comprising: electrically biasing a bit line associated with the at least one memory cell, opening a word line associated with the at least one memory cell, and destructively reading data stored in the at least one memory cell.